WHAT IS CLAIMED IS:

1. A solid-state imaging apparatus comprising:

a solid-state imaging device including a light receiving portion having a plurality of light receiving pixels, a storing portion arranged adjacent to the light receiving portion, and a horizontal transfer portion arranged adjacent to the storing portion;

a timing control circuit for dividing a first clock having a predetermined cycle to generate a vertical scan timing signal and a horizontal scan timing signal;

a vertical drive circuit connected to the timing control circuit for generating a vertical transfer clock from a second clock, the cycle of which is shorter than the first clock, in accordance with the vertical scan timing signal, wherein the vertical transfer clock is used to transfer information charges accumulated in the light receiving pixels of the light receiving portion to the storing portion; and

a horizontal drive circuit connected to the timing control circuit for generating a horizontal transfer clock from the first clock in accordance with the horizontal scan timing signal, wherein the horizontal transfer clock is used to output the information charges transferred from the storing portion to the horizontal transfer portion.

2. The solid-state imaging apparatus according to claim 1, further comprising a dividing circuit connected to the timing control circuit for generating the first clock by dividing the second clock.

3. The solid-state imaging apparatus according to claim 2, wherein a dividing ratio of the second clock in the dividing circuit is variably set in accordance with the information

charge storing time of the solid-state imaging device.

4. A method for driving a solid-state imaging device including a light receiving portion having a plurality of light receiving pixels, a storing portion arranged adjacent to the light receiving portion, and a horizontal transfer portion arranged adjacent to the storing portion, the method comprising the steps of:

dividing a reference clock with a predetermined dividing ratio to generate a divisional clock having a cycle longer than the cycle of the reference clock;

generating a vertical scan timing signal and a horizontal scan timing signal from the divisional clock;

generating a vertical transfer clock from the reference clock in accordance with the vertical scan timing signal;

providing the vertical transfer clock to the light receiving portion and the storing portion in order to transfer information charges accumulated in the light receiving pixels of the light receiving portion to the storing portion;

generating a horizontal transfer clock from the divisional clock in accordance with the horizontal scan timing signal; and

providing the horizontal transfer clock to the horizontal transfer portion in order to output the information charges transferred from the storing portion to the horizontal transfer portion.

5. The driving method according to claim 4, further comprising a step of varying the predetermined dividing ratio in accordance with the information charge storing time of the solid-state imaging device.